Efficient Sum of Absolute Difference Computation on FPGAs

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Martin Kumm, Marco Kleinlein and Peter Zipf
University of Kassel, Germany
Sum of Absolute Difference (SAD)

- SAD is an important operation in image and video processing
- Metric to measure the distance between two blocks of an image
- Applications are, e.g., motion estimation or stereo matching
- An $R \times C$ SAD operation of two matrices $A$ and $B$ is defined as:

$$SAD(A, B) = \sum_{i=1}^{R} \sum_{j=1}^{C} |a_{i,j} - b_{i,j}|$$
Previous Work

Sequential AD [1]

Parallel AD [2]

FPGA optimized [3]

- SAD is computed with $N$ absolute difference (AD) units
- $N$-input adder tree/compressor tree required
- LUTs of best reported circuit grow with $2.5NB$ ($B$: word size)
Proposed SAD

- SAD is computed with $N/2$ 1x2 SAD units
- $N/2$-input adder tree / compressor tree required
- LUTs of proposed SAD grow with $2.0NB$ ($B$: word size)
Results

(a) Required and estimated LUTs

(b) Relative LUT reduction compared to [3]
Check out *uni_ks* git branch of https://scm.gforge.inria.fr/anonscm/git/flopoco/flopoco.git

See you at the poster at 3:30!

**Literature:**