An Evaluation on the Accuracy of the Minimum Width Transistor Area Models in Ranking the Layout Area of FPGA Architectures

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Motivation

- Increasing FPGA based SOC designs
- Reconfigurable fabrics benefit applications
- Non-FPGA companies may use FPGA fabric
- Accurate estimation of layout area
- Early floorplanning
Current Area Model

Drawback – wiring & diffusion sharing not considered

Area in terms of $\lambda$
$16\lambda \times 13\lambda = 208\lambda^2$
VPR Area Model

Area(x) = 0.5 + 0.5x

Area in terms of λ

when x = 1; 1 mwt -> 208λ²
x = 2; 1.5 mwt -> 312λ²
COFFE Area Model

- **nMOS transistors**
  - \( \text{Area}(x) = 0.447 + 0.128x + 0.391\sqrt{x} \)

  \[\text{when } x=1 ; 0.97 \text{ mwt } -> 200.93\lambda^2\]

- **CMOS transistors**
  - \( \text{Area}(x) = 0.518 + 0.127x + 0.428\sqrt{x} \)

  \[\text{when } x=1 ; 1.07 \text{ mwt } -> 223.18\lambda^2\]
FPGA building blocks

- nMOS based Components
  - Encoded and Decoded Multiplexers

- CMOS based Components
  - Buffers
  - Full adders

Models accuracy at ranking different FPGA architectures?
Encoded Multiplexer

- 2:1 LUT
- 4:1 Encoded Multiplexer
Decoded Multiplexer

- 8:1 Decoded Multiplexer
- two level multiplexer
2:1 Multiplexer

Two discrete transistors

Transistors with diffusion sharing

w_{eff} = 1
Effect of folding on area

<table>
<thead>
<tr>
<th>Transistor size</th>
<th>without folding</th>
<th>with 2 folds</th>
<th>with 3 folds</th>
</tr>
</thead>
<tbody>
<tr>
<td>4x</td>
<td>600(\lambda^2)</td>
<td>680(\lambda^2)</td>
<td>802 (\lambda^2)</td>
</tr>
<tr>
<td>6x</td>
<td>792(\lambda^2)</td>
<td>840(\lambda^2)</td>
<td>952(\lambda^2)</td>
</tr>
<tr>
<td>10x</td>
<td>1176(\lambda^2)</td>
<td>1160(\lambda^2)</td>
<td>1250(\lambda^2)</td>
</tr>
<tr>
<td>12x</td>
<td>1368(\lambda^2)</td>
<td>1320(\lambda^2)</td>
<td>1400(\lambda^2)</td>
</tr>
</tbody>
</table>
Transistors with small drive strengths

\[
\text{Active Area}_{2:1\text{mux}} = (9 + 4w_{\text{eff}})24 \lambda^2
\]
Transistors with large drive strengths

minimum width transistor area

\[(4n+1)4\lambda\]

minimum adjacent transistor spacing

\[w_{\text{eff}}(4\lambda) / n\]
\[ \text{Active Area}_{2:1mux} = \frac{(9n + 4w_{\text{eff}})(2n + 1)8}{n} \lambda^2 \]

**Note, if \( n=1 \), the above equation is the same as previous equation**

\[ \text{Active Area}_{2:1mux} = \frac{(9n + 4w_{\text{eff}})(2n + 1)8\lambda^2}{n \times 208\lambda^2} \quad \text{mwt} \]

\[ (9n + 4w_{\text{eff}})(2n + 1) = \frac{26n}{26} \quad \text{mwt} \]

**Differentiating with respect to \( n \)**

\[ \frac{\partial \text{Active Area}_{2:1mux}}{\partial n} = \left( \frac{18}{26} - \frac{4w_{\text{eff}}n^2}{26} \right) \quad \text{mwt} = 0 \]

\[ n^2 = \frac{4w_{\text{eff}}}{18} \]

\[ n = \left[ \frac{\sqrt{2w_{\text{eff}}}}{3} \right] = 0.471\sqrt{w_{\text{eff}}}, n \geq 1 \]

\( n \) is the number of folds of transistor with drive strength \( w_{\text{eff}} \).

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Everyone Makes a Mark
Layout Strategy
Layout strategy for decoded multiplexer

2:1 mux
Buffers - Multistage Buffer

diffusion sharing
Full adder

schematic

layout
Results

- Active area comparison
- Layout area
  - number of metals used
  - Encoded & Decoded multiplexer
    - 1x transistor size
    - change in transistor size
  - CMOS based components
    - buffers and full adder
Active area calculation

- **Encoded Multiplexer**

\[ \text{Active Area}_{k-LUT} = (2^k - 1) \text{Active Area}_{2:1mux} \]

- **Decoded Multiplexer**

\[ \text{Active Area}_{z:1 \ dmux} = \left( \frac{z}{2} + 1 \right) \text{Active Area}_{2:1mux} \]

- \( k \) is the number of inputs to LUT

- \( z \) is the number of inputs to decoded multiplexer
Active area comparison – Part I

VPR: overestimates
33% to 139%

COFFE: overestimates
for 1x - 6x transistor sizes 14% to 29%
- very close for large transistor sizes

Active Area - Encoded and Decoded Multiplexers

Difference

Transistor size

VPR
COFFE
VPR: - underestimates 1x inverter 4%
   - overestimates larger inverters, buffers & full adder 72%

COFFE: - underestimates for inverters 18%
   - overestimates for full adder 46%
Full layout area metal layers

**Example**: INTEL 45nm Metal Stack

<table>
<thead>
<tr>
<th>Layer</th>
<th>thickness(nm)</th>
<th>width(nm)</th>
<th>pitch(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M9</td>
<td>7 µm</td>
<td>17.5 µm</td>
<td>30.5 µm</td>
</tr>
<tr>
<td>M8</td>
<td>720</td>
<td>400</td>
<td>810</td>
</tr>
<tr>
<td>M7</td>
<td>504</td>
<td>280</td>
<td>560</td>
</tr>
<tr>
<td>M6</td>
<td>324</td>
<td>180</td>
<td>360</td>
</tr>
<tr>
<td>M5</td>
<td>252</td>
<td>140</td>
<td>280</td>
</tr>
<tr>
<td>M4</td>
<td>216</td>
<td>120</td>
<td>240</td>
</tr>
<tr>
<td>M3</td>
<td>144</td>
<td>80</td>
<td>160</td>
</tr>
<tr>
<td>M2</td>
<td>144</td>
<td>80</td>
<td>160</td>
</tr>
<tr>
<td>M1</td>
<td>144</td>
<td>80</td>
<td>160</td>
</tr>
</tbody>
</table>
Encoded & Decoded Multiplexer

- Change in transistor size

4:1 encoded mux

4:1 decoded mux

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### Multiplexers – 1x transistor size

#### Total Layout Area Comparison Transistor $\text{weff}=1$

<table>
<thead>
<tr>
<th>Metal</th>
<th>Multiplexer Type</th>
<th>min</th>
<th>max</th>
<th>net variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 metal</td>
<td>Encoded</td>
<td>56%</td>
<td>59%</td>
<td>3%</td>
</tr>
<tr>
<td>2 metal</td>
<td>Encoded &amp; Decoded</td>
<td>37%</td>
<td>59%</td>
<td>22%</td>
</tr>
<tr>
<td>3 metal</td>
<td>Encoded</td>
<td>43%</td>
<td>54%</td>
<td>11%</td>
</tr>
<tr>
<td>3 metal</td>
<td>Encoded &amp; Decoded</td>
<td>22%</td>
<td>54%</td>
<td>32%</td>
</tr>
</tbody>
</table>

**VPR**

- VPR - 2metals
- VPR - 3metals
- COFFE - 2metals
- COFFE - 3metals
Multiplexers – 1x transistor size

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<td>Encoded</td>
<td>57%</td>
<td>60%</td>
<td>3%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded</td>
<td>39%</td>
<td>60%</td>
<td>21%</td>
</tr>
<tr>
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<td>Encoded</td>
<td>45%</td>
<td>56%</td>
<td>11%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded</td>
<td>25%</td>
<td>56%</td>
<td>31%</td>
</tr>
</tbody>
</table>
Effect of transistor size

**Total Layout Area Comparison - Transistor \( \text{weff}=6 \)**

<table>
<thead>
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<th>Multiplexer Type</th>
<th>min</th>
<th>max</th>
<th>net variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 metal</td>
<td>Encoded 1x</td>
<td>56%</td>
<td>59%</td>
<td>3%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 1x</td>
<td>37%</td>
<td>59%</td>
<td>22%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 6x</td>
<td>-59%</td>
<td>18%</td>
<td>77%</td>
</tr>
<tr>
<td>3 metal</td>
<td>Encoded 1x</td>
<td>43%</td>
<td>54%</td>
<td>11%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 1x</td>
<td>22%</td>
<td>54%</td>
<td>32%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 6x</td>
<td>-54%</td>
<td>31%</td>
<td>85%</td>
</tr>
</tbody>
</table>
## Effect of transistor size

### Total Layout Area Comparison - Transistor \( \text{weff}=6 \)

<table>
<thead>
<tr>
<th>Metal</th>
<th>Multiplexer Type</th>
<th>min</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Encoded 1x</td>
<td>57%</td>
<td>60%</td>
<td>3%</td>
</tr>
<tr>
<td>2 metal</td>
<td>Encoded &amp; Decoded 1x</td>
<td>39%</td>
<td>60%</td>
<td>21%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 6x</td>
<td>27%</td>
<td>60%</td>
<td>33%</td>
</tr>
<tr>
<td>3 metal</td>
<td>Encoded 1x</td>
<td>45%</td>
<td>56%</td>
<td>11%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 1x</td>
<td>25%</td>
<td>56%</td>
<td>31%</td>
</tr>
<tr>
<td></td>
<td>Encoded &amp; Decoded 6x</td>
<td>19%</td>
<td>56%</td>
<td>37%</td>
</tr>
</tbody>
</table>

### Diagram

- **VPR - 2 metals**
- **VPR - 3 metals**
- **COFFE - 2 metals**
- **COFFE - 3 metals**

**Legend**

- **2- LUTor 4:1 dmux**
- **3-LUT**
- **4-LUT**
- **8:1 dmux**

**Difference**

- 40%
- 20%
- 0%
- -20%
- -40%
- -60%
FPGA CMOS Components

Total Layout Area Comparison - CMOS Components

- VPR
- COFFE

<table>
<thead>
<tr>
<th>Difference</th>
<th>1x inverter</th>
<th>2x inverter</th>
<th>4x buffer</th>
<th>16x buffer</th>
<th>full adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPR</td>
<td>-50%</td>
<td>34%</td>
<td>84%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COFFE</td>
<td>-51%</td>
<td>13%</td>
<td>64%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Circuit topology and wiring demand differs for CMOS components
Conclusion

- **Minimum width transistor area model**
  - analyzed for commonly used FPGA components
    - **VPR underestimates**: encoded multiplexers and small size buffers
    - **overestimates**: decoded multiplexers with large transistor sizes, large size buffers and full adders.
    - **COFFE underestimates**: buffers and encoded and decoded multiplexers
    - **overestimates**: full adders.

- **Variation in area is due to**
  - different components have different circuit topologies

- **Accurate FPGA area model**
  - consider connectivity and grouping of adjacent transistors
  - component by component area model
Thank You.